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Abstract: This paper addresses the behavioural modelling of digital integrated circuit buffers for performance assessment of high-speed data links. A new modelling technique, with several important advantages is described. All the requirements of black-box identification are met: the approach relies exclusively on the observation of the external port voltages and currents, thus allowing the extraction of models that mimic the operation of real devices without insight on their internal structure. Furthermore, unlike the standard algorithms currently used in EDA tools, the method described in this paper provides a straightforward solution to modelling the input-output behaviour. Good model performance in overclocking conditions is an important advantage. The paper also investigates the possibility of accounting for power-supply voltage variations and provides a simple solution.

1. Introduction

Nowadays, the design of modern electronic equipment requires the assessment of system performance in the very early design phase. Such an assessment, which is mainly achieved via the numerical simulation of interconnected structures, is aimed at predicting the transient evolution of the analogue signals flowing on system interconnects to detect possible malfunctioning and to promptly apply design corrections [1-4]. In this framework, the availability of numerical models describing the external behaviour of digital integrated circuits (ICs) is of paramount importance.

IC ports act as nonlinear dynamical terminations for the interconnects at various levels within an electronic system (on printed circuits boards for example as shown in Fig. 1), thus strongly influencing the shape of signals on the interconnects themselves. Transistor-level descriptions are seldom available since they disclose confidential information on the internal structure and technology of devices. Even when provided by IC suppliers, in encrypted form, they lack portability, turn out to be greedy in terms of processor cycles and cannot effectively be used in a simulation environment. Owing to this, the best compromise is the development of behavioural models, that attempt to mimic the port electrical behaviour of devices (e.g., see Fig. 2a) and that can be effectively estimated from the observation of the signals at the IC interfaces.

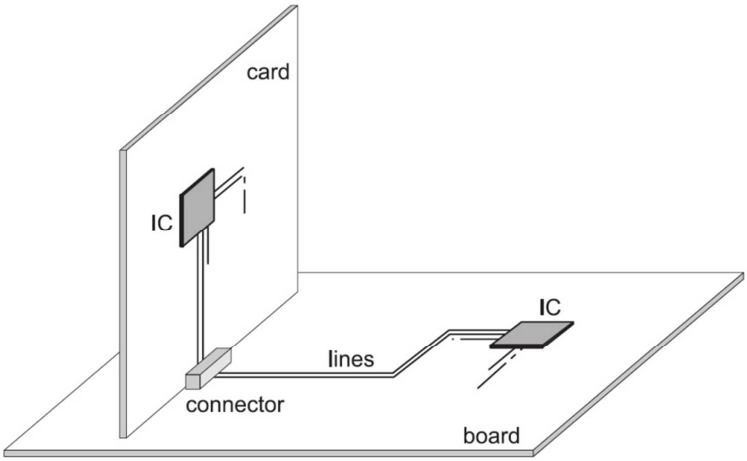

Fig. 1. *Example of interconnect system on a printed circuit board.*

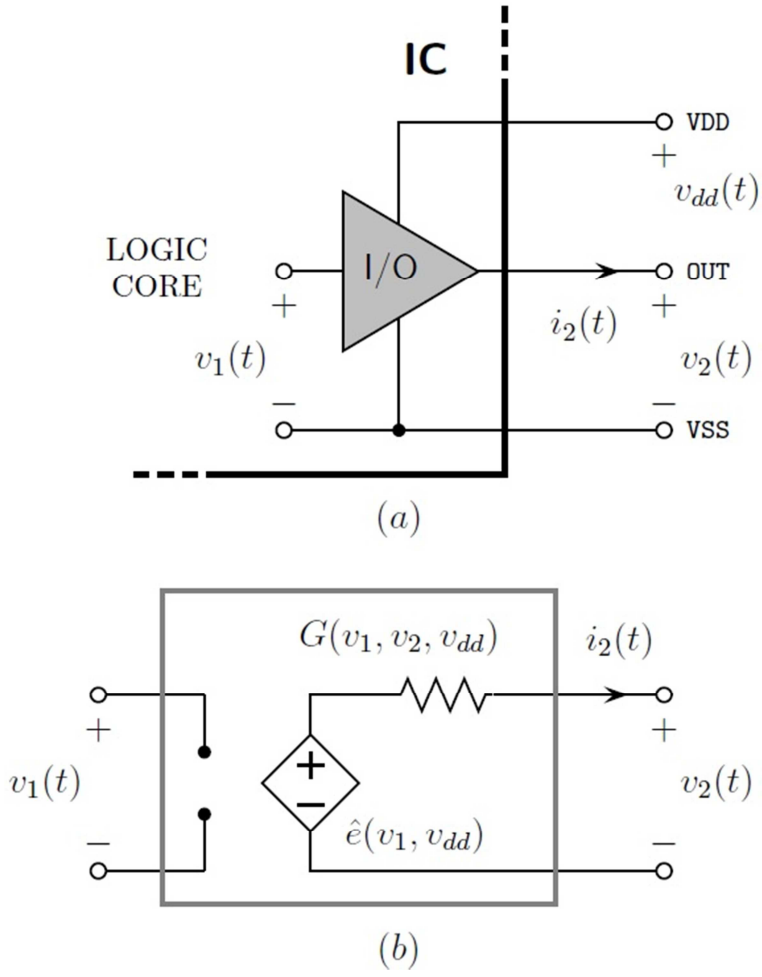

Fig. 2. *a) Typical structure of a digital IC with the relevant electric variables b) Generalized Thevenin mode .*

The standard solution in IC buffer modelling is offered by the Input/Output Buffer Information Specification (IBIS). IBIS assumes simplified equivalent circuits of typical buffer structures and provides guidelines for collecting the key features of devices (e.g., the static characteristics of the output port of a

buffer, the equivalent capacitance of the silicon die, the parameters of the equivalent circuit of the package,...) [5-6]. Recently, other approaches that complement IBIS and provide improved accuracy for recent device technologies have been proposed [7-14].

However, all the state-of-the-art approaches share common limitations. The switching behaviour of devices is not always accurately reproduced; models often have troubles mimicking overclocking operation or spurious transition events. In some cases models have a very complex structure and cumbersome algorithms are used for parameter estimation.

2. IC Buffer Modelling

Consider the single-ended CMOS buffer in Fig. 2a. It represents the basic structure of the I/O interfaces between the internal core circuitry to the external interconnects. Any model of such a device needs to implement a nonlinear dynamic mathematical relation binding the port voltage to the current variables, e.g. $i_2 = F(v_1, v_2)$. Nevertheless, most of the available models are built around a simpler paradigm $i_2 = F(v_2)$, where a system of weighting functions is used to account for the influence of the input voltage. This simplification facilitates the computation of model parameters from both simulation and measurement (e.g., see [7] and [8]) but may lead to inaccuracies, specifically in the case of overclocking-related phenomena.

A Texas Instruments 8-bit bus transceiver (model name SN74ALVCH16973, nominal power supply voltage $VDD = 2.5\,\mathrm{V}$) is used as an illustrative example throughout the paper. Its SPICE transistor level description is available on the vendor's official website and was used to compute the reference waveforms.

The power supply voltage $v_{dd}(t)$ is considered constant throughout sections 3, 4 and 5 of the paper. Section 6 is specifically dedicated to modelling power-supply variations and all issues related to the topic are discussed therein.

3. Generalized Thevenin Model

In the proposed approach the Thevenin-like structure of Fig. 2b is used, where $\hat{e}(v_1)$ is the open circuit voltage response of the buffer to the input voltage v_1 and $G(v_1, v_2)$ is a nonlinear conductance. In a more general case a nonlinear admittance element could be used instead in order to take into account the dynamic behaviour of the output port, mainly the output capacity, but for the sake of a simpler illustration of the method a purely static circuit element was considered in this paper. This assumption may appear restrictive, but it is justified in light of the accurate results shown in the following sections. In addition, it

allows a simpler understanding of how the model structure relates to state-of-the-art methodologies and what its advantages are. As a further refinement, $G(v_1, v_2)$ may be modelled by a nonlinear dynamical element, without modifying the general theoretical framework provided in this paper.

The estimation of model parameters amounts to determining $\hat{e}(v_1)$ and the characteristic curve of the nonlinear conductance $G(v_1, v_2)$ from device responses. In order to facilitate parameter estimation from both simulation and measurement, the series conductance is assumed to be defined by:

$$\begin{aligned} G(v_1, v_2) &= w_H G_H(v_2) + w_L G_L(v_2) \\ &= \left(\frac{\hat{e}(v_1)}{VDD}\right) G_H(v_2) + \left(1 - \frac{\hat{e}(v_1)}{VDD}\right) G_L(v_2) \end{aligned} \qquad (1)$$

where $G_H(v_2)$ and $G_L(v_2)$ are the nonlinear conductances associated to the fixed high and low output state, respectively. The equation above is a two-piece relation accounting for the change of the output buffer's impedance with respect to the variation of the input signal driving the buffer. Note that (1) uses $\hat{e}(v_1)$ as a weighting function that accounts for switching. This is consistent with the physics of CMOS circuits. During switching events the output current is intrinsically weighted by the gate voltage which in turn is related to the open circuit-output voltage.

The first issue that needs to be addressed is the modelling of $\hat{e}(v_1)$. Ideally, an EDA tool should implement a general solution. IBIS-based tools use concatenated, properly trimmed, pre-recorded voltage curves describing typical up-down and down-up transitions in order to simulate drivers for arbitrary input signals. The open circuit voltage $\hat{e}(v_1)$ could be reconstructed in the exact same manner. However, this approach, while being robust, is also responsible for the inaccurate behaviour observed in IBIS models used in overclocking conditions. Indeed, overclocking has become a topic of significant interest among modellers.

The authors chose to use a variant of the classical Hammerstein approach depicted in Fig. 3. The open circuit voltage $\hat{e}(v_1)$ is modelled as a cascade of three blocks. The first block is purely static and consists in a table-based model simply mapping the static open-circuit input-output characteristic of the buffer. The second block is a linear filter and the third block is an ideal delay line accounting for the measured delay of the device in open circuit.

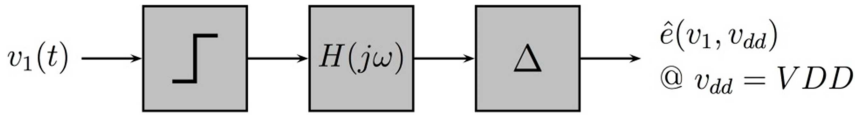

Fig. 3. *Block diagram illustrating the model of voltage- controlled power source* $\hat{e}(v_1)$

The only block requiring the use of elaborate identification tools is the linear filter. Indeed, this block needs to be compact and to accurately mimic the device's input-output dynamic behaviour. Literature provides a wide range of possible approaches and the authors chose to rely on the well-known vector-fitting algorithm [15] in its relaxed version [16]. This technique is known to be robust, reliable and is readily available to potential users. The required input data consists in a set of *n* samples of the frequency-domain response (i.e. $H(j\omega)$ for $\omega = \omega_0, \omega_1, ..., \omega_n$). A cleverly cast least squares problem and an iterative pole-relocation algorithm are then used to compute a rational approximation of $H(j\omega)$. Convergence is generally fast, requiring less than 10 iterations. It should be noted that the order of the filter, which corresponds to the total number of poles included in the rational approximation, depends on the desired accuracy vs. speed trade-off. However, given its simple structure, this type of system is very efficiently handled by SPICE tools even at higher orders. A detailed presentation of vector fitting is beyond the scope of this paper, one can refer to [15], [16] and the references therein for additional information.

Fig. 4 shows the open circuit response of the driver as well as that of the model to an input waveform featuring spurious transition events. With a normalized mean square error of -38.13 dB the predicted response proves remarkably accurate. The order of the linear filter used in this case was 4, amounting to a very compact model.

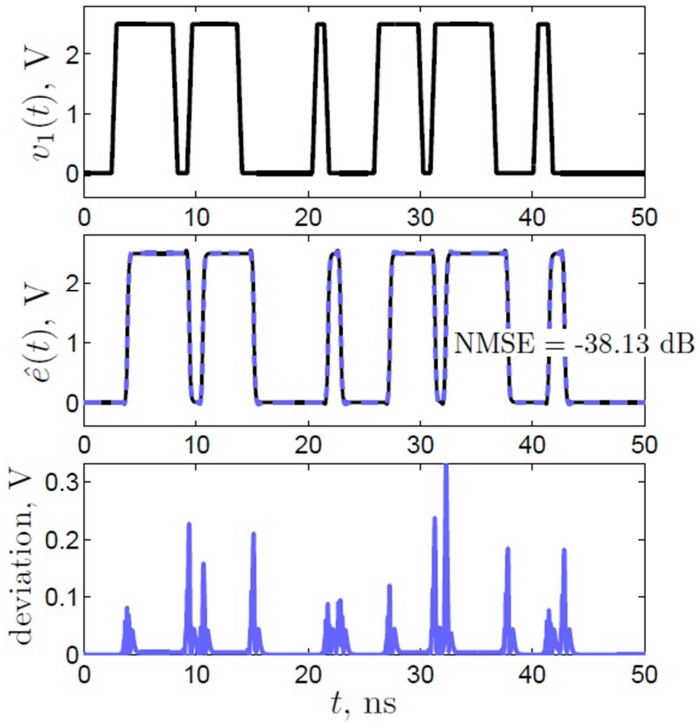

Fig. 4. *Top panel: input voltage (random bit stream). Bottom panel: transient open circuit responses of the real device (solid line) and of the model (dashed line).*

The second issue concerns conductances $G_H(v_2)$ and $G_L(v_2)$ of (1) (see Fig. 5). These are determined via a DC analysis with an ideal voltage source v_2 connected to the output port of the buffer. The buffer is locked in high or low state respectively, and the conductances are computed via Ohm's law according to $G_{H,L} = i_2 / (\hat{e}(v_1) - v_2)$ and simply embedded in the SPICE netlist of the model as tables.

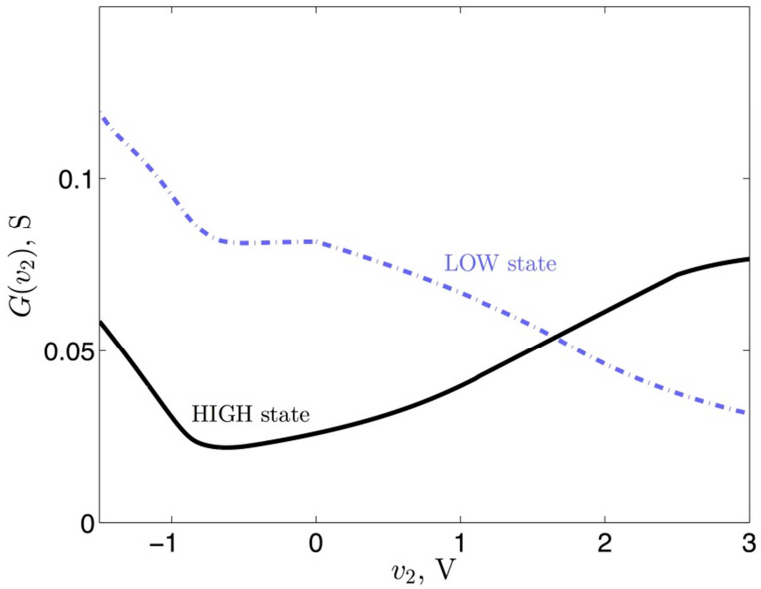

Fig. 5. *Nonlinear conductance as a function of v_2 and of the operating state of the buffer.*

It is relevant to remark that model parameters, i.e. $\hat{e}$ and $G_{H,L}$, can also be computed from actual measurements performed on a real device, with standard solutions for the test fixture.

The overall Thevenin-like model extraction algorithm is summarized below and graphically illustrated in Fig. 6.

1) With the driver in open circuit, run a DC sweep of v_1 in order to extract the static input-output characteristic $v_2(v_1)$ and implement the first block in figure 3. This is a simple two column table that can be easily embedded in a SPICE sub-circuit.

2) Run a transient simulation of the driver, in open circuit, using a step stimulus for v_1. Measure the delay exhibited by the v_2 response and extract it. Compute the derivative of the un-delayed (shifted) step response and, subsequently, obtain the frequency response $H(j\omega)$ by simple FFT.

3) Use vector-fitting to obtain a rational fit of the frequency response $H(j\omega)$ of the filter and generate the equivalent SPICE model. Embed the delay by using an ideal transmission line. At the point $\hat{e}$ is completely modelled.

4) Run two DC sweeps on the driver output port with the device locked in on and off state respectively in order to extract the $i_2(v_2)$ characteristics.

5) Compute G_H, and G_L, from the $i_2(v_2)$ characteristics using Ohm's law, embed the results as tables in spice sub-circuit. At this point both elements of the Thevenin-like circuit are fully modelled.

It's worth noting that steps 2) and 3) could be modified to allow a direct identification in time domain using time-domain vector fitting [17]. On a more general level, the Thevenin-like model in Fig. 2b. could be implemented in various ways. The identification of the $\hat{e}(v_1)$ block, for example, is a classical single-input-single-output dynamic system identification problem and a plethora of methods is available in academic literature: neural networks, polynomial filters or various heuristics (e.g., see [18-20]). The authors preferred the Hammerstein approach for its straightforward implementation but also because the static characteristic of the device, which is of paramount importance, is modelled in accurate and explicit fashion.

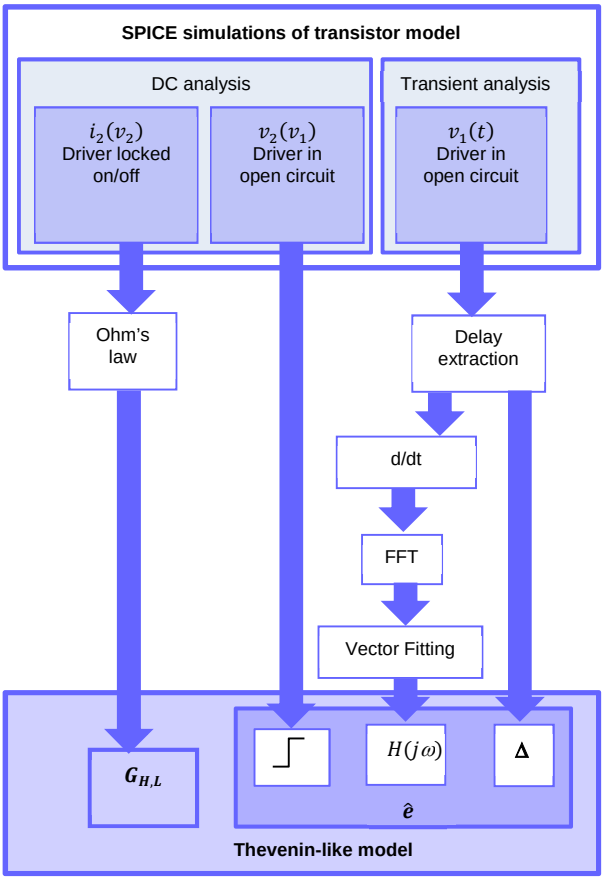

Fig. 6. *Flow chart illustrating the algorithm described in section 3.*

4. Simulation results

In this section, the Thevenin-like model is used to simulate a realistic interconnect structure consisting of the driver connected to a distributed load defined by a transmission line with a 60 Ohm characteristic impedance and 100 ps delay. The transmission line is terminated by a lumped equivalent of a receiver circuit represented by the shunt connection of a 7 pF capacitor.

The input waveform is the same as the one in Fig. 4. The responses of the driver, of the Thevenin-like model and of an IBIS model are shown in Fig. 7. There is a very good agreement between the Thevenin response and the reference while the IBIS response exhibits misalignment phenomena each time a spurious transition occurs.

This is not surprising, the crop-and-paste IBIS strategy has an intrinsic problem at high frequencies and this is precisely the issue that the Thevenin approach presented here addresses.

The waveforms in Fig. 7 were generated on a standard computer with an *Intel(R) Core(TM) i5* processor and 4 GB RAM. A 10× speed-up was recorded for the Thevenin-like model with respect to the

reference. This further confirms the strength of the proposed method and it's worth noting that the speed-up is independent of the complexity of the original transistor model.

The eye diagram is one of the most efficient validation tools in the field of system integrity. Fig. 8 provides comparative eye diagrams for the reference driver and the Thevenin-like model using clock signals at three different frequencies: 333, 606 and 827 MHz respectively. A transmission line load with a characteristic impedance of 75 Ohm and a delay of 400 ps terminated on a 1pF far end capacitor in parallel with a 200 Ohm resistor was used. The match between the diagrams is almost perfect at lower frequencies and retains remarkable accuracy as the frequency increases. Note that at 827 MHz the driver is functioning in overclock conditions. Some signal integrity parameters have been collected in Table I for the three clock signals. Rise and fall times are defined with respect to thresholds accounting for 20% and 80% of the step height.

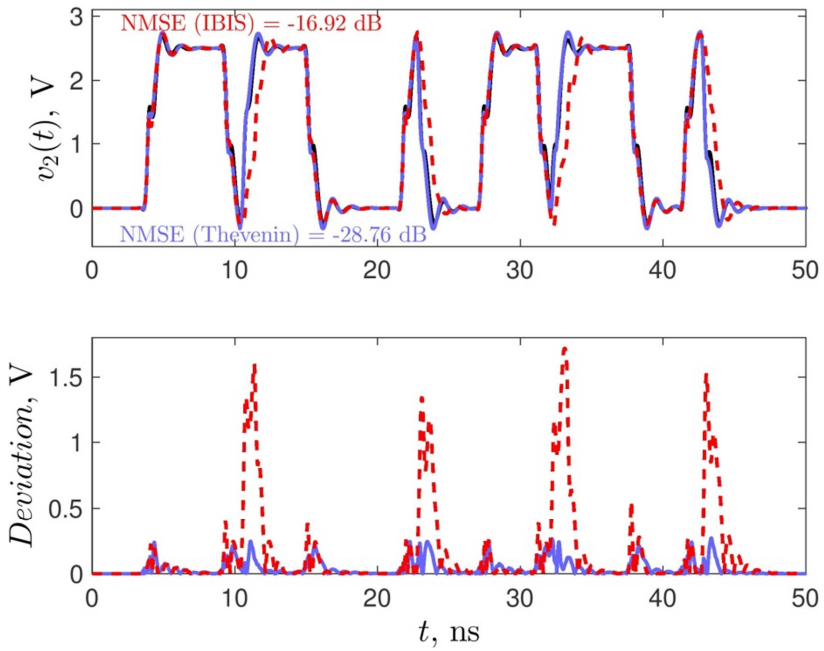

Fig. 7. *Output port voltage response of the example buffer loading an transmission line with 60 Ohm characteristic impedance, 0.1 ns delay and a far end 7 pF capacitor. Solid black: reference response; solid blue: Thevenin model prediction; dashed red: IBIS model prediction.*

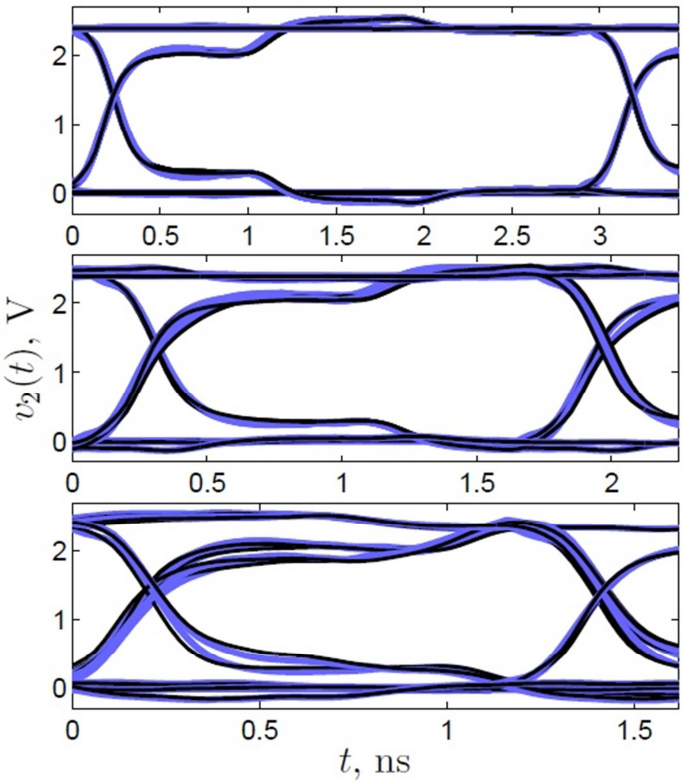

Fig. 8. *Eye diagrams comparing the driver response (solid black) and the model response (blue) at 333 MHz (top panel), 606 MHz (middle panel) and 827 MHz (bottom panel).*

Table 1 Signal integrity parameters for the transistor model and the Thevenin-like model at different frequencies

	333 MHz		606 MHz		827 MHz	
	Ref.	Mod.	Ref.	Mod.	Ref.	Mod
Rise time (ns)	0.335	0.307	0.334	0.307	0.335	0.307
Fall time (ns)	0.228	0.232	0.229	0.222	0.314	0.265
Overshoot (V)	2.526	2.524	2.534	2.524	2.550	2.562
Undershoot (V)	-0.145	-0.140	-0.115	-0.122	-0.155	-0.168

5. Relation to previous approaches

In IBIS models (or models generated by similar techniques such as [7-9]) the output current of the buffer writes:

$$i_2(t) = \tilde{w}_H(t)\,\tilde{f}_H(v_1, v_2) + \tilde{w}_L(t)\,\tilde{f}_L(v_1, v_2) \qquad (2)$$

where $\tilde{f}_H(v_1,v_2)$ and $\tilde{f}_L(v_1,v_2)$ are the static characteristics of the output port of the buffer in the fixed high and low state, respectively, and $\tilde{w}_{H,L}(t)$ are weighting functions that are computed numerically from the device responses on two resistive loads via the solution of a least-squares problem (e.g., see [5] or [6] for details). This is also true for alternative approaches such as [8] or [9].

The first advantage of the technique described in the present paper is the use of the structure in Fig.3. This is a sound and accurate analytical model describing the input-output behaviour of the buffer while remaining SPICE-friendly, simple and robust. The importance of this issue was already recognized by the authors of [12]. Their approach was to use two coupled structures, each similar to the one in Fig. 3, to model the pre-driver stage of a buffer. While leading to very accurate models, the method breaks away from the requirements of black-box modelling because it requires information on internal circuit nodes. Furthermore it may not be used for some buffer architectures. These issues were circumvented by the solution proposed in this paper which also turns out to be more compact.

Now consider Fig. 2b and equation (1). In this case, the expression of the output current can be cast as follows:

$$\begin{aligned} i_2(t) &= G(v_1,v_2)(\hat{e}(v_1)-v_2) \\ &= w_H(t)(\hat{e}(v_1)-v_2)G_H(v_2)+w_L(t)(\hat{e}(v_1)-v_2)G_L(v_2) \\ &= w_H(t)\,f_H(v_1,v_2)+w_L(t)\,f_L(v_1,v_2) \end{aligned} \quad (3)$$

Clearly, equations (2) and (3) are similar and it is interesting to note that the top-down approach of the authors (from circuit theory to macromodel) finally leads to a paradigm similar to the IBIS one obtained by a bottom-up approach (from transistor model to macromodel). Yet another difference appears when carefully comparing (2) and (3). In the case of the IBIS-based models, the two submodels $\tilde{f}_H$ and $\tilde{f}_L$ of (2) only account for fixed high and low state nominal values of the input, namely *VDD* and 0 respectively. The same holds for the approaches described in [8] or [9] which seek to maximize accuracy by relying on improved, dynamic submodels. Instead, in the case of the Thevenin-like model, the inclusion of $\hat{e}(v_1)$ in f_H and f_L provides a stronger link to the input port when switching actually occurs, and the model, more reactive, is more successful in mimicking the overall dynamic behaviour of the circuit.

6. Inclusion of the power supply variation

In this section a simple way of modelling the influence of the power-supply voltage on the output signal is considered.

The power supply voltage $v_{dd}(t)$ is seen as an independent aggressor source acting on the output current i_2. The objective is to capture both fast variations due mostly to electromagnetic compatibility issues and slow deviations from the nominal value due to the supply itself and the structure of the Thevenin-like model allows a straightforward approach.

Let VDD denote the nominal value of $v_{dd}(t)$ and let the open circuit voltage $\hat{e}(v_1, VDD)$ be modelled according to the algorithm described in section III. It can be assumed that the influence of $v_{dd}(t)$ on the actual switching threshold voltage is small and that the problem is mostly a matter of amplitude matching. A general model of $\hat{e}(v_1, v_{dd})$ may be simply and efficiently built following equation (4)

$$\hat{e}(v_1, v_{dd}) = \frac{\hat{e}(v_1, VDD)}{VDD} v_{dd} \qquad (4)$$

The influence of the power supply voltage on the behaviour of a single-ended driver locked in off-state is negligible, thus one may consider G_L as independent from $v_{dd}(t)$. This is not the case when the driver is in on-state. A simple way of accounting for this dependence is a linear correction under the form

$$G_H(v_1, v_{dd}) = a(v_{dd}) G_H(v_1, VDD) + b(v_{dd}) \quad (5)$$

where $G_H(v_1, VDD)$ is simply the nonlinear conductance computed in section III.

The practical implementation simply requires DC analysis to be performed for various values in a given range around VDD. Coefficient vectors a and b can subsequently be obtained by simple polynomial fitting and embedded in the model as tables. The technique is basic but quite effective as long as $v_{dd}(t)$ variations remain within reasonable limits. Fig. 9 illustrates the approach for a random bit stream and a realistic $v_{dd}(t)$ waveform exhibiting impulse noise commonly associated with switching phenomena. With a normalized error of -30.03 dB the match between the model response and the

reference is remarkably accurate The nominal value of the power supply voltage for the example driver was 2.5 V. Being able to perform signal integrity assessments accounting for $v_{dd}(t)$.

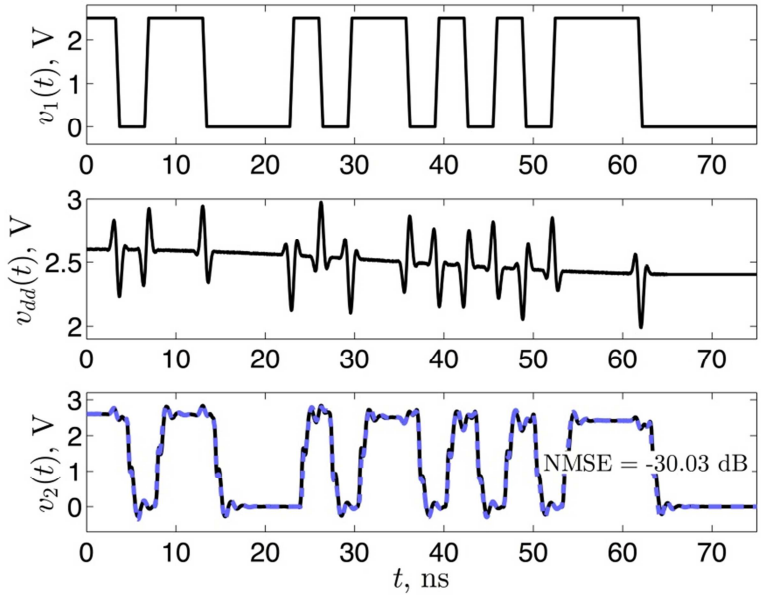

Fig. 9. *Input voltage (upper panel), v_{dd} variation (middle panel) and driver response(lower panel); transistor model response in solid black, Thevenin-like model response in dashed blue.*

7. Conclusions

This paper presents an original paradigm in IC buffer black-box modelling. The concept is based on a generalization of the Thevenin equivalent circuit and, interestingly enough, is mathematically related to the existing IBIS paradigm. The overall buffer model is made up of very simple building blocks, static mappings, an ideal delay line, a low order linear filter. It is easy to derive and implement using commonly available software. The strength of the method resides in the novel way of assembling these building blocks and is well illustrated by the accurate results and the significant speed-up. Device operations are accurately reproduced even during spurious state transitions or overclocking. Furthermore the input-output characteristic of the device is mathematically modelled in a simple and efficient way thus offering a far more flexible solution than the crop-and-paste approach currently used in IBIS-based software. The possibility of including power supply variations has also been explored in the final section of the paper.

Hence, this study provides a reliable basic framework for future EDA tools. Furthermore, the approach is flexible and versatile and subsequent enhancements should easily fit on the established framework. Such enhancements may include additional model blocks accounting for higher order output port dynamics, model customizations accounting for specific device technologies or for environment-dependent parameters such as temperature.

8. References

[1] M.B. Yelten, T. Zhu, S. Koziel, P.D. Franzon, 'Demystifying Surrogate Modeling for Circuits and Systems', IEEE Circuits and Systems Magazine, 2012, **12**, (1), pp. 45-63.

[2] E.-P. Li, X.-C. Wei, A.C. Cangellaris, E.-X. Liu, Y.-J. Zhang, M. D'Amore, J. Kim and T. Sudo, 'Progress Review of Electromagnetic Compatibility Analysis Technologies for Packages, Printed Circuit Boards, and Novel Interconnects', IEEE Trans. on Electromagnetic Compatibility, 2010, **52**, (2), pp. 248-265.

[3] M. Swaminathan, D. Chung, S. Grivet-Talocia, K. Bharath, V. Laddha and J. Xie, 'Designing and Modeling for Power Integrity', 2010, IEEE Trans. on Electromagnetic Compatibility, **52**, (2), pp. 288-310.

[4] I. S. Stievano, I. A.Maio, F. G. Canavero, 'Macromodeling of differential drivers', IET Circuits, Devices & Systems, Feb. 2007, **1**, (1) pp. 34-40.

[5] A.K. Varma, M. Steer, P.D. Franzon, 'Improving Behavioral IO Buffer Moldeing Based on IBIS', IEEE Transactions on Advanced Packaging, 2008, **31**, (4), pp. 711-721.

[6] T. Zhu, P.D. Franzon, 'Application of surrogate modeling to generate compact and PVT-sensitive IBIS models', Proc. of the 18th IEEE Conference on Electrical Performance of Electronic Packaging and Systems(EPEPS), Portlant USA, Oct. 2009, pp . 77 - 80.

[7] T. Zhu, M. B. Steer and P. D. Franzon, 'Accurate and Scalable IO Buffer Macromodel Based on Surrogate Modeling', IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011, **1**, (8), pp. 1240-1249.

[8] I. S. Stievano, I. A. Maio, F. G. Canavero, 'Mπlog, Macromodels via Parametric Identification of Logic Gates', IEEE Transactions on Advanced Packaging, 2004, **27**, (1), pp. 15-23.

[9] B. Mutnury, M. Swaminathan and J.P. Libous, 'Macromodeling of nonlinear digital I/O drivers', IEEE Transactions on Advanced Packaging, 2006, **29**, (1), pp. 102-113.

[10] Y. Cao, R. Ding, Q.-J. Zhang, 'State-Space Dynamic Neural Network Technique for High-Speed IC Applications: Modeling and Stability Analysis', IEEE Transactions on Microwave Theory and Techniques, 2006, **54**, (6), pp. 2398-2409.

[11] Y. Cao, Q.-J. Zhang, 'A New Training Approach for Robust Recurrent Neural-Network Modeling of Nonlinear Circuits', IEEE Transactions on Microwave Theory and Techniques, 2009, **57**, (6), pp. 1539-1553.

[12] W. Dghais, T. R. Cunha, J. C. Pedro, 'A Novel Two-Port Behavioral Model for I/O Buffer Overclocking Simulation', IEEE Trans. Compon., Packag. Manuf. Technol. , 2013, **3**, (10), pp. 1754 - 1763

[13] W. Dghais, T. R. Cunha, J. C. Pedro, 'Reduced-order Parametric Behavioral Model for Digital Buffers/Drivers with Physical Support', IEEE Trans. Compon., Packag. Manuf. Technol., 2012, **2**, (12), pp. 1-10.

[14] Y. Cao, I. Erdin, Q.-J. Zhang, 'Transient Behavioral Modeling of Nonlinear I/O Drivers Combining Neural Networks and Equivalent Circuits', IEEE Microwave and Wireless Components Letters, 2010, **20**, (12), pp: 645-647.

[15] B. Gustavsen and A. Semlyen, 'Rational approximation of frequency domain responses by vector fitting', IEEE Trans. Power Delivery, 1999, **14**, (3), pp. 1052-1061.

[16] B. Gustavsen, 'Relaxed Vector Fitting Algorithm for Rational Approximation of Frequency Domain Responses', Proc. of the 10th IEEE Workshop on Signal Propagation on Interconnects (SPI), Berlin, Germany, May 2006, pp.97-100.

[17] S. Grivat-Talocia, 'Package Macromodeling via Time-Domain Vector Fitting', IEEE Microw. and Wireless Comp. Lett., 2003, **13**, (11), pp. 472-474.

[18] S. Haykin, Neural Networks - A Comprehensive Foundation. Englewood Cliffs, NJ: Prentice Hall, 1999.

[19] M. G. Telescu, I. S. Stievano, F. G. Canavero, N. Tanguy, 'An Application of Volterra Series to IC Buffer Models', Proc. of the 14th IEEE Workshop on Signal Propagation on Interconnects (SPI), Hildesheim, Germany, May 2010, pp. 93-96.

[20] C. Diouf, M. Telescu, N. Tanguy, P. Cloastre, I.S Stievano, F.G Canavero, 'Statically constrained nonlinear models with application to IC buffers', Proc. of the 15th IEEE Workshop on Signal Propagation on Interconnects (SPI), Naples, Italy, May 2011, pp.115-118.