Maintenance Testing of Mixed-Signal Boards

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Abstract

In the context of maintenance and diagnosis of faulty boards, we introduce a functional FSM[1]-based model for mixed-signal circuits. We target efficient test sequences generation for ATE[2] based on a high-level, functional modeling of components assemblies. The approach is flexible, allows to handle digital as well as analog and mixed-signal components in a similar way. A primary prototype has been developped, and two industrial cases partially processed.

Keywords

Modeling, maintenance testing, functional testing, mixed-signal boards, ATPG[3].

1 Introduction

Numerous test methods and techniques have been developped for circuit test [1, 2], associated to the different stages of product lifecycle, mainly at design and production levels. In this paper, we focus on the maintenance phase of mixed-signal boards. At this step, the goal is to check the board behavior, and to determine and replace faulty components in case of defective functionality. Checking and diagnosis imply applying test vectors to the board primary inputs and analyzing outputs as compared to good-known responses. For diagnosis of faulty components, internal measurement points have also sometimes to be defined. Depending on the different cases, engineers have to face various situations for generating ATE programs, ranging from BIST-equiped, well-documented components to blackbox-like ones. In the later case, methods developped for the production phase cannot be used since boards have no associated test capabilities or informations.

At least partially automated test generation has well known advantages. It increases productivity, reduces cost, and helps to manage complex (e.g. large mixed-signal) boards testing. Automated test pattern generation rests upon models for both the board components and the faults to be detected. It can also be associated to metrics for measuring the effectiveness of the tests. Many component and fault models are based on structural or physical representations of the device under test. Unfortunatly, as mentioned previously, such informations are not always available in the maintenance context.

[1]Finite State Machine
[2]Automatic Test Equipment
[3]Automatic Test Pattern Generation

Since they make only use of the external behavior of the components, functional-based models can address a wide spectrum of situations concerning testing for board maintenance: they can be adapted to the amount of information available (component specification levels), to the nature of the components (digital, mixed, or analog) and to the goal of the test (go-nogo, fine-grain diagnosis oriented testing).

However, even if these are attractive for component modeling, functional models lack associated fault models, and thus ATPG methods and fault coverage metrics.

To deal at least partially with these disadvantages, we present in the following section our FSM-based functional models for the components and tests of mixed-signal boards. We decline these models according to the type of components and the availability of functional specifications. There is no specific fault model. Instead, since specifications are based on FSM, functional coverage is obtained by states and transitions coverage of the FSM. First results are briefly presented next.

2 Board modeling for ATPG

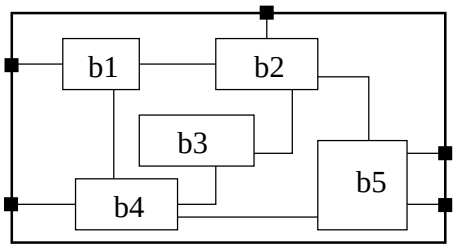

Figure 1: A board is an assembly of blocks

The target board can be seen as an assembly of *components* or *blocks* as depicted in picture 1. The global test consists in testing each block individually using an associated *test model*. This test model is created by merging a block *functional model* and a *test strategy* as depicted in the central part of the picture 2. Test vectors for a component are generated by covering each transition of the component's test model. Since the block under test is often embedded within the system, without any test access mechanism (e.g. block b3 of picture 1), the functional models of adjacent components are used for justification and propagation of the block I/O up to the system boundaries. Vectors are computed using constraint logic programming.

The proposed approach for the functional modeling of the components is based on communicating FSM, since these objets are part of engineers background, flexible enough to handle various kinds of board specifications, with graphical aspects. Moreover, covering the test model may simply consist in covering each of its nodes and transitions.

We detail next more precisely the role of each model in the ATPG process, and how these models can be automatically generated in some cases.

The functional model of each component is a set of communicating FSM. A tool has been developped for the graphical input of such specifications from scratch [3]. This tool is to be used mainly for the modeling of specific digital components. For a given component, there could exist alternative FSM-based representations. In particular coarse-grain or fine-grain representations of the functionality of a block are possible, and lead to different covering rates in terms of detailed functionalities. This flexibility is mandatory since functional aspects to be handled in a maintenance context can vary considerabily, due to deliberated test engineer directives, or to the lack of information at disposal.

Instead of expressing directly the FSM model with appropriate tools, at least three other ways of specification are possible, as shown on the left side of picture 2:

- Library components – mainly common analog and mixed-signal blocks, like filters, comparators, converters – can be chosen. The associated functional model is generated automatically taking

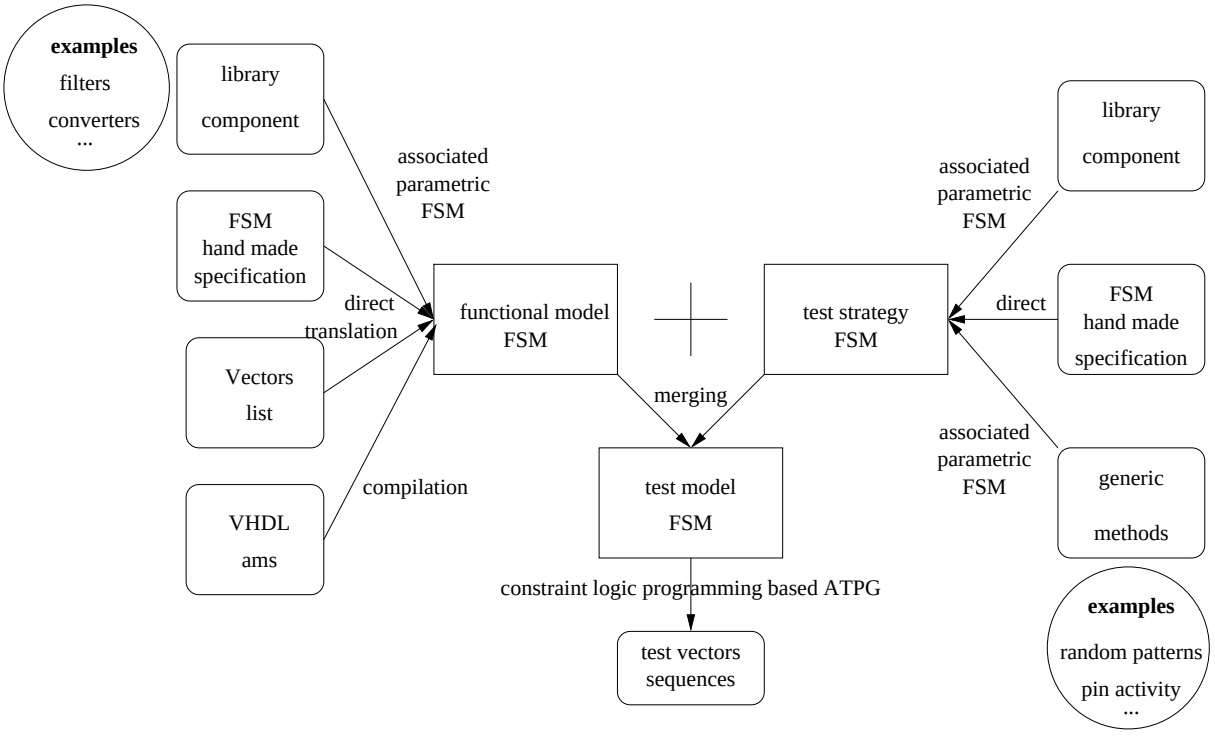

Figure 2: The test method process flow

into account some parametric aspects (e.g. threshold levels, linearity, tolerance rate, ... for comparators).

- VHDL/AMS subset specifications for the description of FSM, as commonly realized for controllers.
- Test vectors lists. These are the simplest way for specifying blackbox-like blocks functionalities. Test vectors are obtained from good-reputed boards.

All of these specification techniques can be mixed, according to the nature of the system components, and to the kind and form of available descriptions for the different blocks. Others specification sources can be added easily, if these can be re-expressed (automatically) as communicating FSM sets. Pre-defined library components have been chosen for some analog and mixed-signal blocks, since this is the simplest way for integrating engineers skills in the analog test field (see the test model paragraph).

The functional model itself is not sufficient for generating suitable test vectors. What are the applicable test generation techniques ? What are the interesting test points of a particular system ? How experimented engineers handle some mixed-signal components ? ... To answer these questions, testing strategies have to be defined and applied to the functional model. We first explain the testing strategy model, before detailing how to exploit it in conjunction with the functional model to obtain a test model.

The test strategy Different strategies can be applied to test a functional model. The right side of picture 2 shows some possibilities for the test strategy:

- For library components, one or more testing strategies can be associated to a component, in the same way as a functional model is stored for a block, with some parametric capabilities. For example, comparators are usually tested with two values on both sides of the threshold + tolerance range.

- More generic methods can also be described by FSM: for example random pattern generation, exhaustive test for blackboxes, pin activity checking, and other classical methods, embedding engineers know-how and skills.
- As for functional models, specific hand-made test strategies, with the largest degree of flexibility to fit test requirements at best.

Since test patterns generation correspond to FSM transitions covering, strategies have to be described as combinations of transitions. As a simplistic example, checking one output pin activity corresponds to some test vectors with 1 and some others with 0 for this pin. The vectors are generated from a FSM containing a transition for the 0-value and a transition for 1-value.

The test model is resulting from the application of the test strategy to the functional model. This is realized mainly by extending the functional model FSM at I/O points, with new FSM pieces implementing the test strategy. For the simplistic example presented previously, we have to augment the functional model with a list of small FSM, at each primary I/O, with 0 and 1 transitions.

As shown at the bottom of picture 2, the test model is used for ATPG. The problem of test data generation is faced using constraint logic programming (CLP) and classical algorithms for finite state machines (transition coverage, state coverage, path coverage). In the prototype, test data are represented in a symbolic way, using ranges of values, dealing efficiently with analog and digital data representation in a uniform way.

Ranges of vectors are computed for reaching the test requirements. Actual values are defined at the end, making possible to take into account some ATE specificities.

3 Conclusion and future work

The approach has been successfully applied for the modeling of two industrial cases. Test vectors have been generated automatically for the first case. Preliminary work for the second case has confirmed the feasibility of the approach. We are currently extending our tool by integrating test strategies. These are to be associated automatically to functional models in order to obtain test models. Thus, we have not only to generate automatically the test vectors from the test model (ATPG part) but also to automate at least partially the test model generation based on the test strategy and functional model of a component. More significant test strategies representations have also to be integrated in the tool. Another objective is to extend the models to take into account more complex systems.

Acknowledgements

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