Equalization of Interconnect Propagation Delay with Negative Group Delay Active Circuits

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Abstract

In this paper, we propose a technique to compensate the propagation delay and losses in VLSI interconnects by using negative group delay (NGD) active circuits. This study uses the RLC models of interconnect lines currently considered in VLSI circuits. The circuit proposed here is based on a cell consisting of a Field Effect Transistor (FET) in parallel with a series RL passive network. We also describe the synthesis method to achieve simultaneously a significant negative group delay and gain. Simulations allow us to first verify the performance of the NGD circuit and also show a restoration of the distorted signal shape as well as a reduction of propagation delay.

I – Introduction

Currently, in deep submicrometer Very Large Scale Integration (VLSI) circuits, the propagation delay of inter-chip interconnect cannot be neglected compared to the gate delays [1]-[2]. The signal integrity is characterized by propagation delays, rise times, overshoots and settling times [3]. Different theoretical approaches have been proposed in various publication to estimate this delay. Among them, the most popular one is the Elmore delay; it is applied to monotonical response systems such as RC models [4]-[5]. For faster on-chip rise times and longer wire lengths, inductance is an important parameter. Then, RLC line models must be used [6]. Recently, Ismail and Friedman [7]-[8] established an accurate expression of the propagation delay intended for the second order system model. The efficiency of these models was evaluated by relative error between exact models using PSPICE tool [9]. The RLC models have proven to be sufficient in the case of signals at frequencies of a few GHz. Here, to compensate the different parasitic effects, we propose a topology of active circuits which exhibits a Negative Group Delay (NGD) in broadband frequencies for base band signals. This circuit consists of a series resistance and inductor in feedback with a field effect transistor.

First, in Section II we will briefly recall the on-chip modeling theory of interconnect lines. Section III will describ the properties of the proposed active topology and present synthesis equations to get NGD in baseband. In Section IV, we will present the simulation results from Agilent-ADS circuit software in frequency- and time-domains when this circuit is associated with interconnect lines modeled by RLC. After discussion on these results, some prospects are presented in the last section.

II –Delay of RC and RLC interconnect models

In 1948, Elmore introduced the 50% propagation delay as:

$$T_{pd} = b_1 - a_1 \qquad (1)$$

for the normalized transfer function [4]:

$$g(s) = \frac{1 + a_1 s + a_2 s^2 + \ldots + a_n s^n}{1 + b_1 s + b_2 s^2 + \ldots + b_m s^m}, \qquad (2)$$

where a_i and b_i are real and $m > n$. For simple RC circuits (fig. 1), this delay is defined as: $T_{dp} = RC$. Furthermore, in 1987, Wyatt [5] introduced this delay as the reciprocal of the dominant pole of the system (3). This delay is exact for simple RC circuits.

$$a_1 = \sum_{i=1}^{n} \frac{1}{z_i} \text{ and } b_1 = \sum_{i=1}^{m} \frac{1}{p_i}, \qquad (3)$$

where z_i and p_i are, respectively, the zeros and the poles of g(s).

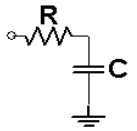


Fig. 1 : RC model.

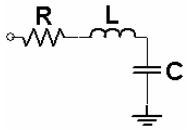


Fig. 2 : RLC model.

At signal frequencies of a few GHz, as the inductance effect cannot be neglected, considering the second-order transfer function is a must. This delay was recently established by Ismail and Friedman [7][8] as being:

$$T_{pd} = 1.047 e^{(\varsigma/0.85)} + 1.39\varsigma, \qquad (4)$$

for the canonical form of the transfer function:

$$g(s) = \frac{\omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2}, \qquad (5)$$

For the RLC circuit in fig. 2, with:

$$\varsigma = \frac{RC}{2\sqrt{LC}}, \qquad (6)$$

and

$$\omega_n = \frac{1}{\sqrt{LC}}. \qquad (7)$$

The phases of these passive circuits are defined as:

$$\varphi_{RC}(\omega) = -\arctan(RC\omega), \qquad (8)$$

and

$$\varphi_{RLC}(\omega) = \arctan\left(\frac{RC\omega}{1 - LC\omega^2}\right). \qquad (9)$$

Then, the group delay $\tau = -\partial\varphi/\partial\omega$ is:

$$\tau_{RC}(\omega) = \frac{RC}{1+(RC\omega)^2}, \quad (10)$$

and $$\tau_{RLC}(\omega) = \frac{RC(1+LC\omega^2)}{1+(CR-2L)C\omega^2+(LC\omega^2)^2}. \quad (11)$$

So, when $\omega \approx 0$: $\tau_{RLC}(0) = \tau_{RC}(0) = RC$. (12)

This delay also occurs for the RC-modeled interconnect lines (fig. 3) driven by the CMOS gate with impedance R_s and loaded also by the next gate with impedance $1/(sC_L)$. The transfer function of this system is expressed as [10]:

$$G(s) = \frac{1}{(1+sR_s)\cosh(\gamma d)+(\frac{R_s}{Z_c}+sC_L Z_c)\sinh(\gamma d)}, \quad (13)$$

where $Z_c = \sqrt{\frac{R+Ls}{Cs}}$ is the characteristic impedance

and $\gamma = \sqrt{(R+Ls)Cs}$ is the propagation constant of the line.

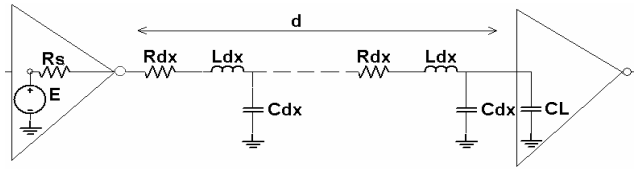


Fig.3: A gate driving an RLC transmission line loaded by the next gate.

III – Topology proposed for NGD active circuits

To compensate for the signal distortion, let us introduce the cell of the circuit presented in fig. 4 where a resistor and an inductor are in feedback with a FET. To simplify the analytical expression, the FET is modeled by the controlled voltage current source; with a transconductance g_m, in cascade with the drain-source resistor R_{ds}.

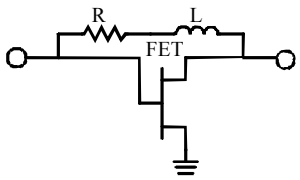


Fig. 4: a unit cell which generates a negative group delay.

The magnitude and phase responses of the transfer function are given by:

$$|G(j\omega)| = R_{ds}\sqrt{\frac{(1-g_m R_{ds})^2+(g_m L\omega)^2}{(R+R_{ds})^2+(L\omega)^2}}, \quad (14)$$

$$\varphi(\omega) = \arctan\left[\frac{L\omega(g_m R_{ds}+1)}{L^2\omega^2 g_m - R_{ds}+(g_m R_{ds}+g_m R-1)R}\right]. \quad (15)$$

Consequently, the group delay $\tau = -\partial\varphi/\partial\omega$ is expressed as:

$$\tau(\omega) = \frac{L(1+g_m R_{ds})((R+R_{ds})(1-g_m R)+g_m(L\omega)^2)}{((g_m R-1)^2+(L\omega g_m)^2)((R+R_{ds})^2+(L\omega)^2)}. \quad (16)$$

It is worth noting that the *existence condition of the negative group delay* is:

$$(R+R_{ds})(1-g_m R)+g_m(L\omega)^2 < 0, \quad (17)$$

and at low frequency, the simplified expression is then:

$$R > \frac{1}{g_m}. \quad (18)$$

So, one can define a pseudo-bandpass where $\tau(\omega)$ remains negative and extracts the root of $\tau(\omega) = 0$ or the cut-off frequency of NGD as:

$$\omega_c = \sqrt{\frac{(R+R_{ds})(g_m R-1)}{L^2 g_m}}. \quad (19)$$

Moreover, if the angular frequency $\omega \approx 0$, it leads to:

$$|G(0)| = \frac{|1-g_m R_{ds}|R_{ds}}{R+R_{ds}}, \quad (20)$$

$$\text{and } \tau(0) = \frac{(1+g_m R_{ds})L}{(R+R_{ds})(1-g_m R)}. \quad (22)$$

By inverting these two relations, R and L can be synthesized separately according to $G(0)$ and $\tau(0)$:

$$R = \frac{(1+|G(0)|)R_{ds}}{g_m R_{ds}-|G(0)|}, \quad (23)$$

$$\text{and } L = -\frac{(1+g_m R_{ds})G(0)\tau(0)R_{ds}}{[g_m R_{ds}-G(0)]^2}. \quad (24)$$

Consequently, relation (23) gives the maximum limit of the gain to guarantee R > 0:

$$|G(0)|_{\max} = g_m R_{ds}. \quad (25)$$

It is worth noting that, curiously, the circuit used in our study (fig. 4) corresponds to the well-known topology of feedback amplifiers. Moreover, the existence of negative group delay as shown by (17) results from an *interaction* between the transistor and the associated passive network. Concerning the

bias circuit, simulations show that it does not disturb the circuit responses. Furthermore, we have established that another association based on a resonant circuit can also produce NGD [11].

Finally, many cells in cascade with the passive circuit are necessary in general to maintain the initial form of the signal.

IV – Simulated results for equalization of propagation delay

The RLC circuit associated with a two-stage active NGD circuit is presented in fig.5. Throughout this study, we used the FET EC2612 (g_m = 98.14 *mS* and R_{ds} = 118.6 Ω).

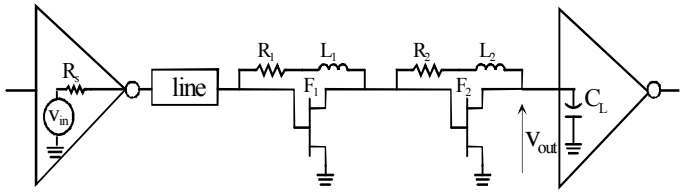
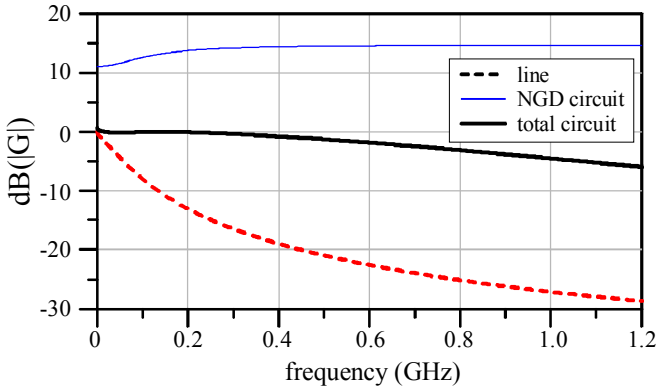


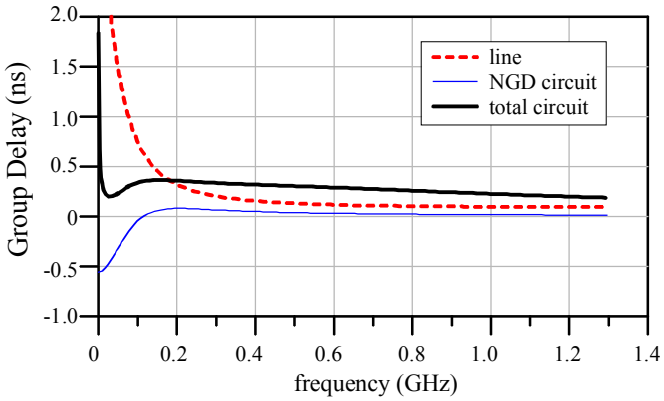
Fig. 5: Combination of the output gate (R_S = 90 Ω), the RLC model line with a two-stage active NGD circuit (F_1 = F_2 = FET EC2612, R_1 = 73 Ω and L_1 = 99 nH, R_2 = 102 Ω and L_2 = 17 nH) loaded by the input capacitor C_L = 30 pF of the next gate.

Figure 6 illustrates the results of the synthesis on magnitude, group delay and time-domain responses of three configurations: the line alone with the two gates (fig. 3), the two-stage NGD circuit with and the whole cascaded circuit (fig. 5). These results are got on condition that the parameters per unit length be R = 76 Ω/cm, L = 5.3 nH/cm and C = 2.6 pF/cm for a length d = 0.8 cm in the Ismail-Friedman RLC longlines model [7].

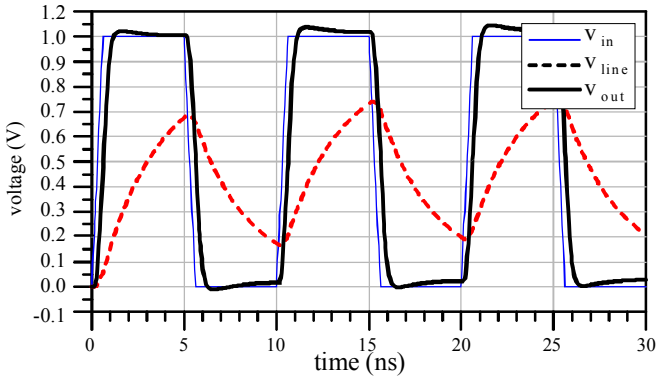
The previously mentioned compensation is confirmed by the time domain simulation shown in fig. 6-c. A trapezoidal signal with a 10 ns period is injected with rise and fall time equal to t_r = 0.6 *ns*. The 50% propagation delay is decreased by 1.60 *ns* and losses are compensated.



(a)



(b)



(c)

Fig. 6- Simulation results (a): Magnitude, (b): group delay and (c): time domain simulation.

V- Conclusions

We described a new topology of a broadband negative group delay active circuit. This circuit allows a reduction of the distortion introduced by interconnect lines such as 50% delay propagation, rise time and attenuation. This result can be obtained thanks to the original properties of NGD phenomenon, which is generated, here, by the interaction between the passive circuit and the FET. Moreover, we established a theoretical method of synthesis and presented some results of frequency- and time-domain simulations in order to show the efficiency of the proposed innovative design. It should be noted that NGD is one of the singular properties of metamaterials, but many cells are necessary to get a significant value. Moreover, inherent strong losses are associated to a narrow band frequency [12]. Here, with a small number of *active* cells, we have obtained significant NGD and loss compensations over a wide frequency band.

The next steps of this study will be a full analytical demonstration of this distortion compensation, an investigation into the noise effects generated by the resistors and the transistors, and determining whether the circuit studied here can be integrated in interconnect on-chips over a wider frequency band.

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