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Experimental Validation of the RC-Interconnect Effect Equalization with Negative Group Delay Active Circuit in Planar Hybrid Technology

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Abstract

This paper deals with the experimental validation of equalization technique of RC-line degradations based on a negative group delay (NGD) active circuit. The feasibility of this method is illustrated by brief theoretical recalls. According to the RC-line parameters, formulas permitting to synthesize this NGD circuit are proposed. Next, experimental results verify the analytical prediction and evidence the efficacy of the technique for prototypes in planar hybrid technology. So, for an input square-wave pulse of 25 Msym/s-rate, the rise-time and the propagation delay of the regarded RC-circuit were respectively reduced by 71.4% and 86.4%. As expected, the recovered measured signal presents an improvement of both raising and trailing edges. Finally, a discussion summarizing the main benefits of this technique compared to the use of repeater is described.

1. Introduction

The last two decades have witnessed the introduction of several new communication services that presented extraordinary challenges to rapid development of microelectronic equipments. This progress is accentuated by the growth of the integration density to hundreds of millions of transistors in a single chip [1]. Nowadays, this makes the interconnect structures more and more complicated. Therefore, their effects notably the time needed for a signal to travel from one part to another part inside the chip can not be neglected [2-3]. Such time assigned as the propagation delay becomes one the main issue in modern VLSI/system-on-chip (SoC) designs. To do so, researches aimed at reporting contributions of these interconnects by proposing simplified models have been performed [4-6]. But the simplest and the most useful is the Elmore one [4] which consists mainly in considering the first order approximation of the transmission line transfer function. This corresponds then to regard the RC-line model. Starting from this simple model, the effects of interconnects which leads to the degradation of signal transitions are limited to time delay and magnitude distortion.

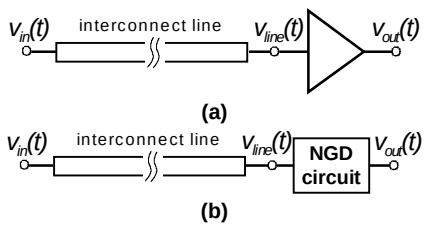

Fig. 1. Interconnect line ended by: (a) a repeater/ (b) an NGD circuit.

To cope with this technological problem, a technique of delay reduction has been introduced in [7-9] using a repeater as schematized in Fig. 1(a). To make more understandable this concept, let us consider a voltage level, V_0. Reminding that according to a threshold level, V_T, a repeater consists in generating an output with either low or high level:

$$v_{out}(t) = \begin{cases} 0 & if \quad v_{line}(t) < V_T \\ V_0 & if \quad v_{line}(t) \geq V_T \end{cases}. \qquad (1)$$

Of course, this technique is inadequate when for example, the signal, $v_{line}(t)$ is highly attenuated and lower than V_T. For this reason, the equalization technique using negative group delay (NGD) active circuit (Fig. 1(b)) was proposed [10-13]. As stated in [11], this NGD equalization technique is ideally aimed at generating an output most likely to the input ($v_{out}(t) \approx v_{in}(t)$). In other word, assuming $G_{line}(s)$ and $G_{NGD}(s)$, the interconnect- and the NGD- transfer functions respectively, it enables to fit that one of the whole structure close to unity:

$$V_{out}(s)/V_{in}(s) \approx 1 \quad \Leftrightarrow \quad G_{NGD}(s)G_{line}(s) \approx 1. \qquad (2)$$

It implies that:

$$|G_{NGD}(j\omega)| \approx 1/|G_{line}(j\omega)|, \qquad (3)$$

and

$$\tau_{NGD}(\omega) \approx 1/\tau_{line}(\omega). \qquad (4)$$

Knowing that $|G_{line}(j\omega)| < 1$ and $\tau_{line}(\omega) > 0$, to achieve this equalization process, the conditions, $|G_{NGD}(j\omega)| > 1$ and $\tau_{NGD}(\omega) < 0$ what justifies logically the use of the NGD active circuit are expected. As seen in Fig. 2, this NGD circuit is composed of a field effect transistor (FET) fed back with an RL series network. To simplify the calculations, the low frequency model of this transistor has been considered.

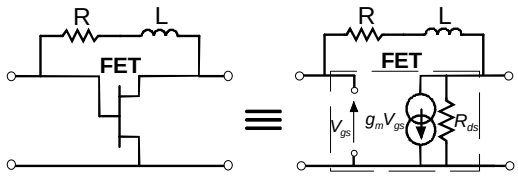

Fig. 2. NGD active cell: FET fed back with an RL series network.

According to the circuit and system theory, losses compensation induced by the gain of the active circuit and an

interconnect group delay reduction can be achieved due to the NGD effect.

The remainder of this paper is structured as follows. In section 2, the theory of RC-line model and the proposed NGD active circuit is recalled prior to describing analytically the interconnect equalization. The next section is consecrated to the validation of the presented technique. It explains the design process of the RC-NGD compensator and explores the measured frequency- and time-domain results. The last section concludes this paper.

2. Theoretical Recalls

To simplify the theory and let us consider that interconnects are modeled by RC-lines as illustrated in Fig. 3.

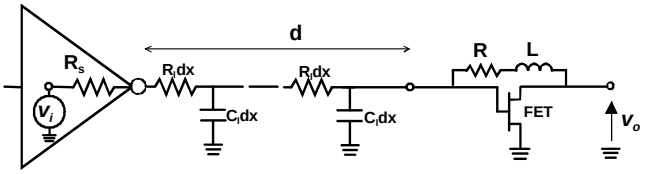

Fig. 3. Gate with output resistance, R_s driving an RC-interconnect line cascaded with an NGD cell.

2.1. RC-line theory

As reported in [7-8], the considered RC-model presents a transfer function given by:

$$G_{RC}(s) = \frac{\sqrt{R_l}}{\sqrt{R_l}\cosh(d\sqrt{R_l C_l s}) + R_s\sqrt{C_l s}\sinh(d\sqrt{R_l C_l s})}. \quad (5)$$

Regarding the first order MacLaurin series expansion of the denominator, this quantity will be reduced as follows:

$$G_{RC}(s) = \frac{1}{1 + (R_s + R_l d/2)C_l ds}. \quad (6)$$

This form of transfer function allows considering an equivalent lumped element RC-circuit with a total resistance and capacitance:

$$R_T = R_s + R_l d/2, \quad (7)$$

and

$$C_T = C_l d. \quad (8)$$

In this case, the Elmore 50% propagation delay [4] is written as:

$$T_{RC} = R_T C_T = (R_s + R_l d/2)\, C_l d. \quad (9)$$

Furthermore, according to the expression (6), this RC-line exhibits a group delay always positive:

$$\tau_{RC}(\omega) = -\frac{\partial \angle G_{RC}(j\omega)}{\partial \omega} = \frac{T_{RC}}{1 + (T_{RC}\omega)^2}. \quad (10)$$

2.2. Recall on the NGD circuit theory

As established in [7], the NGD cell shown in Fig. 1 presents a transfer function expressed as:

$$G_{NGD}(s) = \frac{R_{ds}(1 - g_m R - g_m Ls)}{R_{ds} + R + Ls}. \quad (11)$$

It is worth reminding that at very low frequency ($\omega \approx 0$), this cell exhibits a gain and a group delay defined as:

$$\left|G_{NGD}(0)\right| = \frac{R_{ds}\left|1 - g_m R\right|}{R_{ds} + R}, \quad (12)$$

$$\tau_{NGD} = -\left.\frac{\partial \angle G_{NGD}(j\omega)}{\partial \omega}\right|_{\omega \approx 0} = \frac{L(1 + g_m R_{ds})}{(1 - g_m R)(R_{ds} + R)}. \quad (13)$$

It means that in base band frequency, losses compensation ($\left|G_{NGD}(\omega)\right| > 1$) and NGD ($\tau_{NGD}(\omega) < 0$) can be achieved under the condition:

$$R > 2R_{ds}/(g_m R_{ds} - 1). \quad (14)$$

2.3. Analytical approach of the proposed RC-line equalization

As stated in [7-8], thanks to the NGD function, interconnect line delay reduction can be realized by considering the configuration shown in Fig. 3. The relevance of this technique is theoretically predicted by the propagation delay expression of this configuration:

$$T = \alpha[(1 + g_m R_T)\tau_{ngd} + T_{RC}], \quad (15)$$

where

$$\alpha = \frac{R + R_{ds}}{R + R_{ds} + R_T(g_m R + 1)} < 1. \quad (16)$$

If $\tau_{NGD} < 0$, T is undoubtedly lower than the RC-propagation delay described by (9). Moreover, knowing the RC-line parameters R_l, C_l and d, we propose the R- and L-synthesis formulas in order to realize the equalization of gain and group delay at very low frequency:

$$R = \frac{2R_{ds} + R_T(g_m R_{ds} + 1)}{g_m R_{ds} - 1}, \quad (17)$$

$$L = \frac{(g_m R - 1)(R + R_{ds})T_{RC}}{g_m^2 R_{ds} R_T + g_m(R_T + R_{ds}) + 1}. \quad (18)$$

These synthesis formulas lead us naturally to experimental investigation devoted in the next section.

3. Experimental Validation of the Proposed Technique

To validate this equalization technique, prototypes of RC-, NGD- and RCNGD-circuits have been designed and tested

both in frequency- and in time-domains. We underline that along this section, the presented design process and simulations were performed with *ADS* designer/simulator from *Agilent*.

3.1. Design Process

To avoid, the eventual disruptions caused by the bias network at low frequency, the FET was biased through application of an improved active-load technique. We use the PHEMT/ATF-34143 from *Avago Technology* because its characteristics, $g_m = 226$ mS and $R_{ds} = 27\ \Omega$ which are extracted from the non-linear model, were well suited for this demonstrator of RC-effects equalization. For the given RC-parameters, the *RL* NGD-circuit values were synthesized via the expressions (17) and (18). Then, accurate frequency responses are obtained through circuit simulations (lumped components and non linear FET model). A final slight optimization was run with the available lumped component values. The layout of the hybrid planar circuit is printed on a FR4 substrate of permittivity, $\varepsilon_r = 4.3$, and thickness, $h = 800$ µm as depicted in Fig. 4.

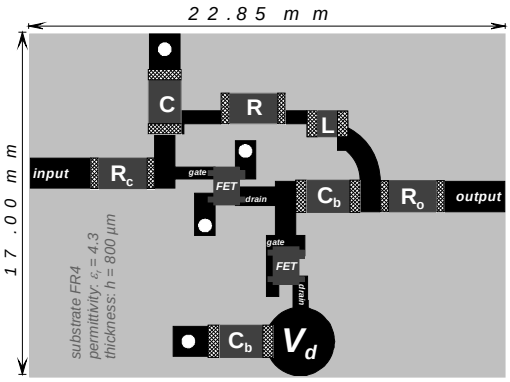

Fig. 4. Layouts of the tested RCNGD-circuit using a PHEMT ATF-34143 ($V_{gs} = 0$V, $V_d = 3$V, $I_d = 110$ mA), for $R_c = 33\ \Omega$, $C = 680$ pF, and $R = 56\ \Omega$, $R_o = 10\ \Omega$, $L = 220$ nH, $C_b = 100$ nF.

3.2. Experimental Results and Discussions

It is emphasized that the frequency and temporal results examined in this subsection were recorded from an *R&S ZVRE 9kHz-4GHz* vector network analyzer and a 2 Gs/s *LeCroy* digital oscilloscope, respectively.

3.2.1. Frequency Results

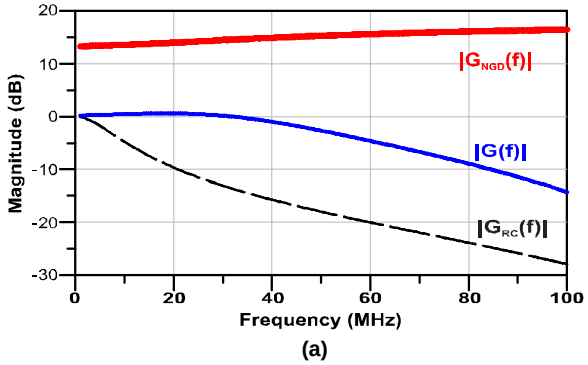

Fig. 5(a). Measured magnitudes of the RC-, NGD- and RCNGD-circuits.

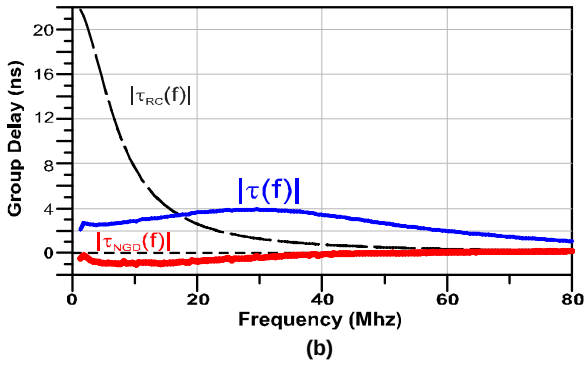

Fig. 5(b). Measured group delays of the RC-, NGD- and RCNGD-circuits.

As plotted in Fig. 5(a), the measured magnitude, $|G(f)|_{dB}$ of the overall circuit is kept within -10 and 0 dB up to 80 MHz and close to 0 up to 40 MHz. It is worth noting that the total magnitude and group delay values are different from the sum of the individual magnitudes because of a possible mismatch between the RC and NGD parts. The group delay of the whole circuit, $\tau(f)$, is not fully cancelled (Fig. 5(b)), but it is kept below 4 ns due to the NGD circuit. An absolute higher NGD value could be theoretically obtained, but a compromise between NGD value, NGD bandwidth and gain flatness has to be found to minimize overshoot or ripple in time-domain.

3.2.2. Time Domain Results

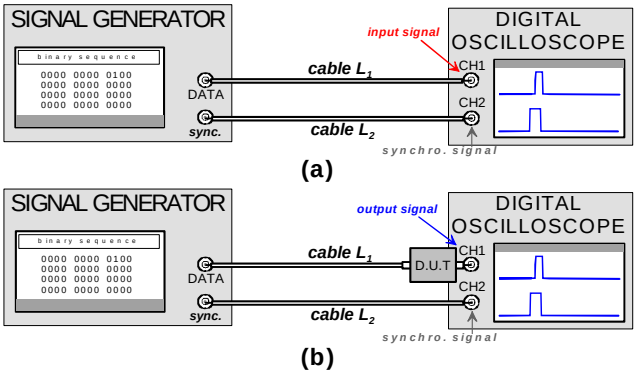

Fig. 6. Schematic diagram of the experimental setup: (a) input and (b) output signal recording.

The executed temporal measurement setup is summarized in Fig. 6. Noticed that the square wave pulse is delivered, at the highest rate available, by the baseband data output of a vector signal generator (*R&S SMJ 100A*). This digital pulse has a 25-Msym/s rate corresponding to a 40-ns width and an amplitude $V_0 = 1$V. As explained in Fig. 6, to avoid cable and connector influences, we proceeded systematically in two steps and recorded, at first, the input and then the output signals (connected on CH1) by using the same synchronization reference signal (connected on CH2). We, thus, monitored the input pulse, V_{in}, the RC- and RCNGD-circuit output ones V_{RC}, V_{RCNGD} which are resynchronized by using the reference signal and plotted in Fig. 7. Compared to V_{RC}, the output V_{RCNGD} waveform is reshaped and less distorted. The RC-circuit provides a degraded output leading edge with $t_{rRC} \approx 35$ ns as rise time and 50% propagation delay of

$T_{RC} \approx 18.50$ ns. Hence, the NGD circuit compensation allowed a reduction of both parameters by leading to $t_{rRCNGD} \approx 10$ ns and $T_{RCNGD} \approx 2.50$ ns, which means relative reductions of 71.4% ($1\text{-}t_{rRCNGD}/t_{rRC}$) and 86.5% ($1\text{-}T_{RCNGD}/T_{RC}$). In addition, as illustrated at the top of Fig. 7, the trailing edge is strongly enhanced. This point is worth being noted when an enhancement of data rate is expected from application of this technique.

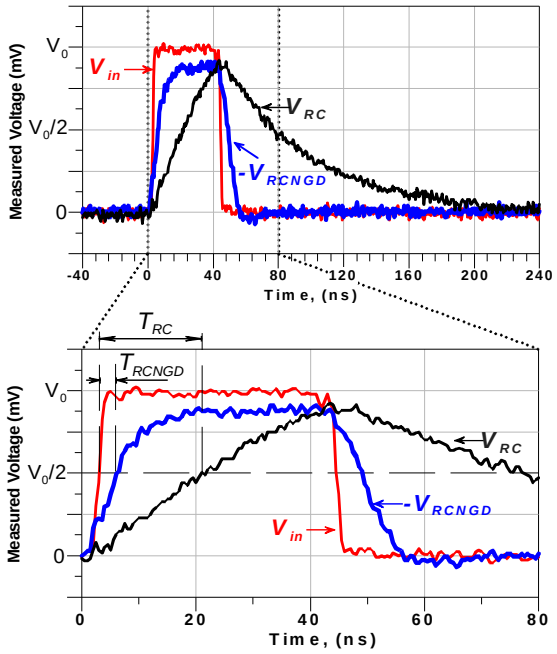

Fig. 7. Time-domain responses with an input square pulse (25-Msym/s rate, 2 ns rise- and fall-times) and zoom on two times of the symbol duration.

3.2.3. Remarks between Repeater and NGD Active Circuit

It is interesting to underline that as reminded aforesaid, regenerative repeaters characterized by their threshold voltages, V_T are sometimes used. Based on the configuration shown in Fig. 1(a), deeming the degraded voltage, V_{RC} plotted in Fig. 7, the lowering level of V_T would also shortening the rise time but similarly, it would increase also the fall time. Thus, this proposition is detrimental to the bit duration. So, it is not actually consistent for systems with high data rate. However, to control simultaneously time delay and back/front edges, a dual threshold voltage repeater of course, with a greater complexity could be proposed. Otherwise, another suggestion could be: "why do not simply amplify before switching to the logical level?" This proposal idea allows also the improvement of the raising edge but it contributes to change again the data duration.

4. Conclusions

A new technique of interconnects (restricted to RC-line) effects equalization is investigated and validated. It consists of cascading the line and an NGD active circuit. It is evidenced theoretically and experimentally that this technique allows enhancing the integrity of the signals degraded and especially the reduction of the propagation delay. To achieve a complete validation and to check the efficacy of the theoretical predictions, the fabricated devices were tested. Indeed, in frequency-domain, the equalization of the RC-circuit magnitude response and the reduction of its group delay were both evidenced. In time-domain, for a 25 Msym/s-rate signal, an excellent reshaping of the degraded signal wave form was obtained. In addition, these measurements confirmed a significant shortening of the rise-time and propagation delay of the distorted signal.

In the continuation of this work, we plan an implementation in MMIC technology. To overcome the eventual difficulty of self integration, investigation on an innovative topology of NGD circuit without inductance is currently in progress.

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