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Application of negative group delay active circuits to reduce the 50% propagation Delay of RC-line model

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Abstract

This paper presents a new method developed to reduce the propagation delay by using a negative group delay (NGD) active circuit. Analytical expressions are proposed to demonstrate the validity of our approach in the case of an RC-transmission line model. The synthesis method of NGD circuits versus the line length is detailed. For a 0.5 Gbit/s digital signal and a 2-cm-long RC-line model, time-domain simulations carried out with a high-frequency circuit simulator showed that the 50% propagation delay was reduced by 94%. Finally, potential applications of this method to compensate for time delays in different interconnect configurations (VLSI, package, on-chip, long-line, ...) are discussed.

I – Introduction

In high-speed applications, time delay has become a major bottleneck in the design process [1]-[3]. This general trend applies to back plane and package interconnects, on-chip and on-board transmission lines, serial or parallel buses and also to VLSI interconnects. For these different domains, various advanced models and robust frequency- and time-domains simulator have been investigated, but the common basic model is the Elmore RC-line one [4]. Starting from this simple model, the effects of interconnects are limited to time delay, magnitude distortion and degraded signal transitions. To enhance the signal integrity, the principle of reduction of these phenomena was put forward in [5] by using a negative group delay (NGD) circuit. Experimental evidences of the negative group delay for both microwave modulated signals and baseband ones were provided in frequency in [6] and in frequency and time-domains in [7]. The topology of NGD cell under study is depicted in fig. 1: it simply consists of a series resistance, R_1 , and an inductance, L_1 , in feedback with a field effect transistor (FET). In a first approximation, this latter is modeled by the transconductance, g_m , in cascade with the drain-source resistor, R_{ds} , as shown in fig. 2. With this topology and for a transmittance, $G(j\omega)$, from the expression of the group delay, $\tau(\omega)$, given in (1) we established in [5] that the group delay, can be negative in a low-pass bandwidth, (when ω tends to 0) under the condition set in (3):

$$\tau(\omega) = -\frac{\partial \angle G(j\omega)}{\partial \omega}, \quad (1)$$

$$\tau_{ngd} = \frac{(1 + g_m R_{ds}) L_1}{(R_1 + R_{ds})(1 - g_m R_1)}, \quad (2)$$

$$1 - g_m R_1 < 0 \Leftrightarrow R_1 > \frac{1}{g_m}. \quad (3)$$

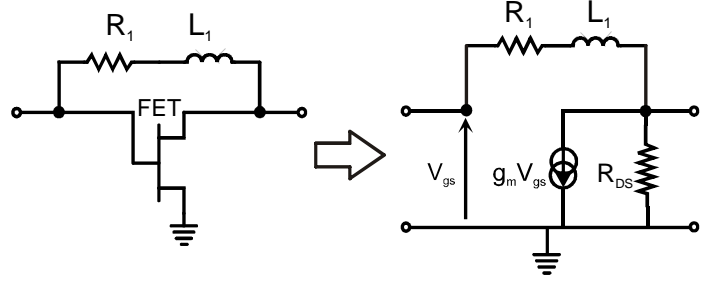


Fig. 1: NGD cell with its simplified equivalent model.

The principle of reduction of interconnect line effects (fig. 2) consists in cascading at the output of the line one or several NGD cells.

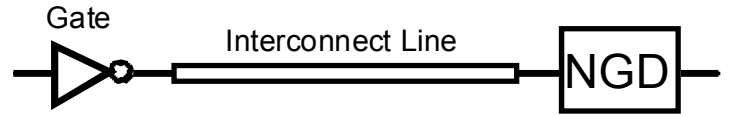


Fig. 2: Block diagram of the compensation technique of interconnect line effects with NGD circuit.

It is worth recalling that the synthesis equations detailed in [5] are about a single cell. But, in practice in the case of high-speed digital signals, several cells must be used to get an NGD value high enough for the desired frequency bandwidth.

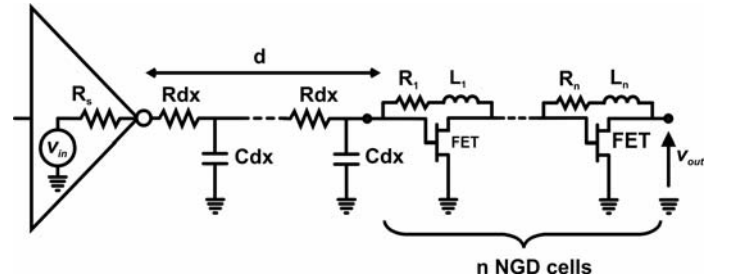


Fig. 3: RC-interconnect line model driven by a gate (output resistance: R_s) and cascaded with n NGD cells.

Let us consider the system presented in fig. 3. The design approach requires to, at first, extract the transfer function and the propagation delay of the interconnect line as a function of its length, d . Then, both of them have to be found in the case

where the line is cascaded with a single NGD cell. Let us now extend the study to the case where n is the optimum number of NGD cells to be cascaded at the output of the interconnect model to compensate for its spurious effects. In Section IV, a synthesis method is proposed to get n versus d . This theoretical approach was completed by time-domain simulations. They showed a 94% reduction of the 50% propagation time delay of a 2-cm-long RC line for a 0.5 Gbit/s rate. At last and before concluding, possible application of this technique to various interconnect configurations are discussed on considering its advantages and drawbacks.

II – Theoretical study of the RC-line model

This section deals with the analytical study of an RC-interconnect line model such as the one in fig. 3. It consists of a gate with an output resistance, R_s , which drives an interconnect RC-line model of length, d , with unit-length resistance, R , and capacitance C . Hence, the characteristic impedance, Z_c and the propagation constant, γ , are defined in the Laplace domain by:

$$Z_c = \sqrt{\frac{R}{Cs}}, \quad (4)$$

$$\gamma = \sqrt{RCs}. \quad (5)$$

Let $V_{in}(s)$ and $V_{out}(s)$ be the Laplace transform of the input- and output- voltages of the circuit with no NGD cells. Then, the quantity $G(s) = V_{out}(s)/V_{in}(s)$ is the transfer function and is expressed as:

$$G_{rc}(s) = \frac{1}{\cosh(\gamma d) + \frac{R_s}{Z_c} \sinh(\gamma d)}. \quad (6)$$

Let us consider the Elmore approach [4] to express the propagation delay. Therefore, for the system under study, by using the first-order Maclaurin expansion of the denominator of (6) and from (4), the approximated transfer function is:

$$G_{rc}(s) = \frac{1}{1 + (\frac{Rd}{2} + R_s)Cs}. \quad (7)$$

Thus, it can be assumed as an RC-circuit with an equivalent resistance, $R_e = R_s + R \times d/2$, and a capacitance, $C_e = C \times d$. As mentioned in [5] and [9], at low frequency ($\omega \rightarrow 0$) the group delay, $\tau(\omega) = -\partial \angle G(j\omega) / \partial \omega$, is also the Elmore propagation delay. It ensues that the Elmore propagation delay is:

$$\tau_{rc} = (\frac{Rd}{2} + R_s)Cd. \quad (8)$$

III – Synthesis method of the NGD cell compensating for the RC-line effects

Let us now focus on the RC-line model of section II cascaded by a single NGD cell (i.e. $n = 1$ in fig. 3 with R_1 and L_1 in feedback). Its transfer function is expressed as:

$$G(s) = \frac{4R_{ds}[1 - g_m(R_1 + L_1s)]}{A(s).(R_{ds} + R_1 + L_1s) + Z_c B(s).(g_m R_{ds} + 1)}, \quad (9)$$

where:

$$A(s) = (3 + 5\frac{R_s}{Z_c})\sinh(\gamma d) + (5 + 3\frac{R_s}{Z_c})\cosh(\gamma d), \quad (10)$$

$$B(s) = (5 + 3\frac{R_s}{Z_c})\sinh(\gamma d) + (3 + 5\frac{R_s}{Z_c})\cosh(\gamma d). \quad (11)$$

To simplify the analytical study, as done above, the first-order term of the equation-(9) denominator expansion is kept; at low frequency, it leads to the magnitude and group delay expressions:

$$|G(0)| = \frac{R_{ds}(g_m R_1 - 1)}{R_1 + R_{ds} + R_e(1 + g_m R_{ds})}, \quad (12)$$

$$\tau_0 = \frac{(R_1 + R_{ds})[(1 + g_m R_e)\tau_{ngd} + \tau_{rc}]}{R_1 + R_{ds} + R_e(g_m R_1 + 1)}. \quad (13)$$

Under condition (3), i.e. $\tau_{ngd} < 0$, it is clear that this propagation delay is lower than the RC-interconnect line one, τ_{rc} , alone (8).

A full compensation of interconnect effects means keeping the output waveform close to the input one, i.e. the transfer function close to unity ($G(s) \approx 1$). Thus, the NGD cell transfer function needs to be the reverse of the line one. From this principle, the synthesis relations of the NGD circuit are established as a function of the line length under the assumptions that $|G(0)| \approx 1$ and $\tau(0) \approx 0$:

$$R_1 = \frac{2R_{ds} + (g_m R_{ds} + 1)R_e}{g_m R_{ds} - 1}, \quad (14)$$

$$L_1 = \frac{(g_m R_1 - 1)(R_1 + R_{ds})\tau_{rc}}{g_m^2 R_{ds} R_e + g_m (R_{ds} + R_e) + 1}. \quad (15)$$

For a realistic line length, d , (15) gives a high inductance value, L_1 , which means that it is better to use n cells of NGD circuit (as shown in fig. 3). Unfortunately, the extraction of synthesis equations for n cells is analytically difficult. So, the next section will be devoted to the development of a pragmatic approach aimed at getting the optimal number of cells to be cascaded at the end of the RC-line of length, d .

IV – Optimization of the NGD cell number and simulation results

To evaluate n , let us calculate the expression of the RC-interconnect line losses as a function of d from the insertion loss formula:

$$L_{dB}(d, \omega) = 20 \cdot \log(e^{\frac{d\sqrt{2RC\omega}}{2}}). \quad (16)$$

The input trapezoidal signal, V_{in} , shown in fig. 4 is defined by its period, T , with a rise/fall time, $t_r = 0.05T$. Such a signal can be characterized by using the significant frequency, f_s , which depends on the ramp time. In [10], f_s was found to be sufficient to represent the signal high-frequency behavior. In fact, 85% of the frequency components of the pulse are within the frequency range set by f_s . Then in [10]-[11], the significant frequency was finally expressed as a function of the clock rate:

$$f_s = 0.35 / t_r = 7 / T. \quad (17)$$

Consequently, in the frequency band from DC up to f_s , the average of the interconnect line losses are:

$$L_{moydB}(d) = 27.15 \sqrt{\frac{RC}{T}} d. \quad (18)$$

To compensate for these losses, let us consider the average in the frequency band defined by f_s of the S_{21} -parameter provided by the FET-manufacturer.

As argued previously, if the length, d , is very long, a single NGD cell may be unable to achieve the compensation. This is why we suggested the use of n cells so that:

$$n = \text{int} \left(\frac{L_{moydB}(d)}{S_{21moydB}} \right), \quad (19)$$

where $\text{int}(x)$ gives the lowest integer equal or higher than x . Fig. 4 is an example of chart for a given RC-model and a specific FET. Fig. 5 shows the schematic of a 2-cm-long line compensated by an NGD circuit with two cascaded cells for values as in fig. 4. For simulations, the output voltages were computed in the time-domain with the *Advanced Design System (ADS)* microwave circuit simulator from *AgilentTM*. Final optimization of the NGD feedback component values led to the results presented in fig. 6.

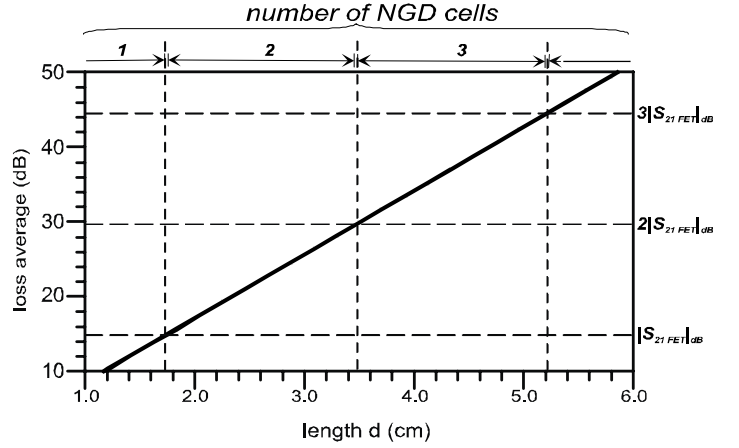


Fig. 4: Optimization of the n NGD cells according to d for $R = 76 \Omega/\text{cm}$ and $C = 2.6 \text{ pF}/\text{cm}$, (FET: EC-2612, $g_m = 98 \text{ mS}$ and $R_{ds} = 117 \Omega$).

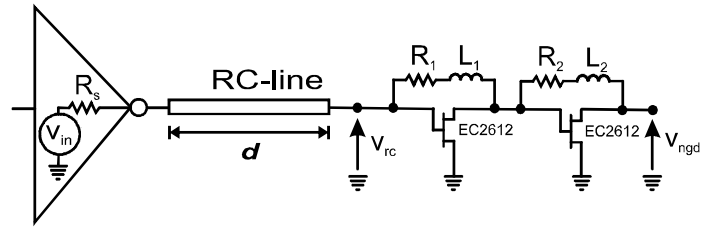


Fig. 5: Schematic of the simulated RC-line ($R_s = 90 \Omega$) compensated by a two-stage NGD circuit ($R_1 = 91 \Omega$, $L_1 = 40 \text{ nH}$, $R_2 = 110 \Omega$, $L_2 = 20 \text{ nH}$)

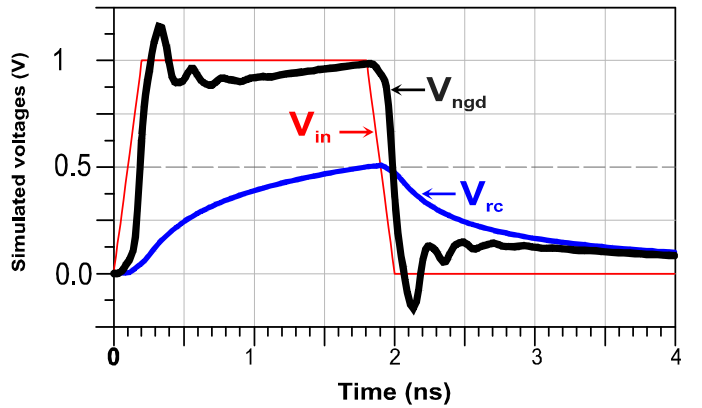


Fig. 6: Input (V_{in}) and output voltages for the RC-line model alone (V_{rc}) and for the overall cascaded system (V_{ngd}).

It shows that, for a trapezoidal input signal at a rate of 0.5 Gbit/s and 200 ps in rise/fall-time, the reduction of the 50% propagation delay for V_{ngd} is about 94% compared to V_{rc} .

V – Discussion on the approach potential and its domain of application

First, one should note that, even with a two-stage circuit, the inductance values remain significant. Moreover, the bias networks generally include inductances. The main drawback is thus the on-chip implementation of such inductances during a classical VLSI process. So, this approach as it is could be applied directly to reduce propagation delay in on-board transmission line or in buses as well as in inter-chip interconnects. But, for the compensation of on-chip interconnect delay, a substitution of inductances (in RL feedback and in bias networks) by an active network as proposed in [12] is worth being considered because of the simplicity of our topology. Other investigations are focused on the search for a new topology with no inductance, but still exhibiting gain and NGD.

VI – Conclusion

Here, we analytically demonstrated that the use of an NGD active circuit permits a reduction of interconnect time delay and described the conditions to be fulfilled. For simplicity reasons, the theoretical developments proposed in this study were about the well-known RC Elmore line model. We also developed synthesis equations suited to the case of an NGD cell cascaded at the end of the line model; in the event that a higher number of NGD cells is needed we also detailed an approach developed to determine the optimum number of cells to be used. Moreover, this approach reduces the inductance to realistic localized component values. In the case of a 2-cm-long RC-line and a high-speed digital input signal, time-domain simulations highlighted the decrease of the spurious effects by using a two-stage NGD circuit. The method limitations and its application to various interconnect configurations were also discussed as well as future prospects.

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